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Jameco Part Number 242763

MC74AC377, MC74ACT377

Octal D Flip-Flop with Clock Enable

The MC74AC377/74ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

- Ideal for Addressable Register Applications
- Clock Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Outputs Source/Sink 24 mA
- See MC74AC273 for Master Reset Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- ACT377 Has TTL Compatible Inputs
- MSL = 1 for all Surface Mount
- Chip Complexity: 292 FETs or 73 Gates

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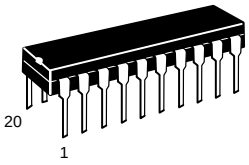
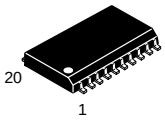
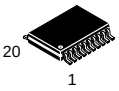
http://onsemi.com



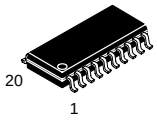
PDIP–20
N SUFFIX
CASE 738



SO–20
DW SUFFIX
CASE 751



TSSOP–20
DT SUFFIX
CASE 948E



EIAJ–20
M SUFFIX
CASE 967

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

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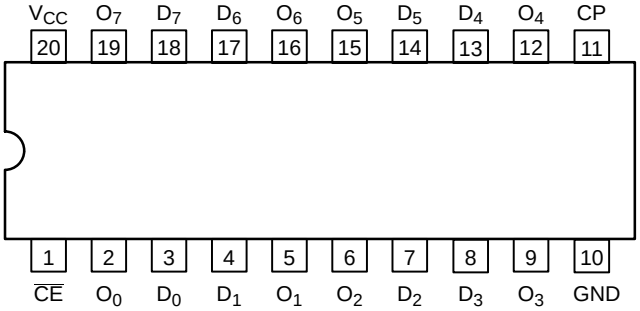


Figure 1. Pinout: 20–Lead Packages Conductors
(Top View)

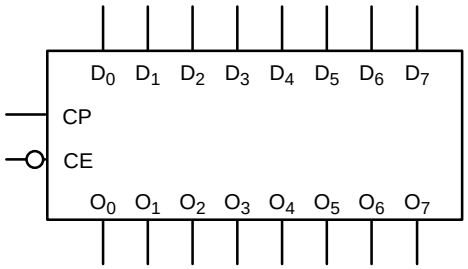


Figure 2. LOGIC SYMBOL

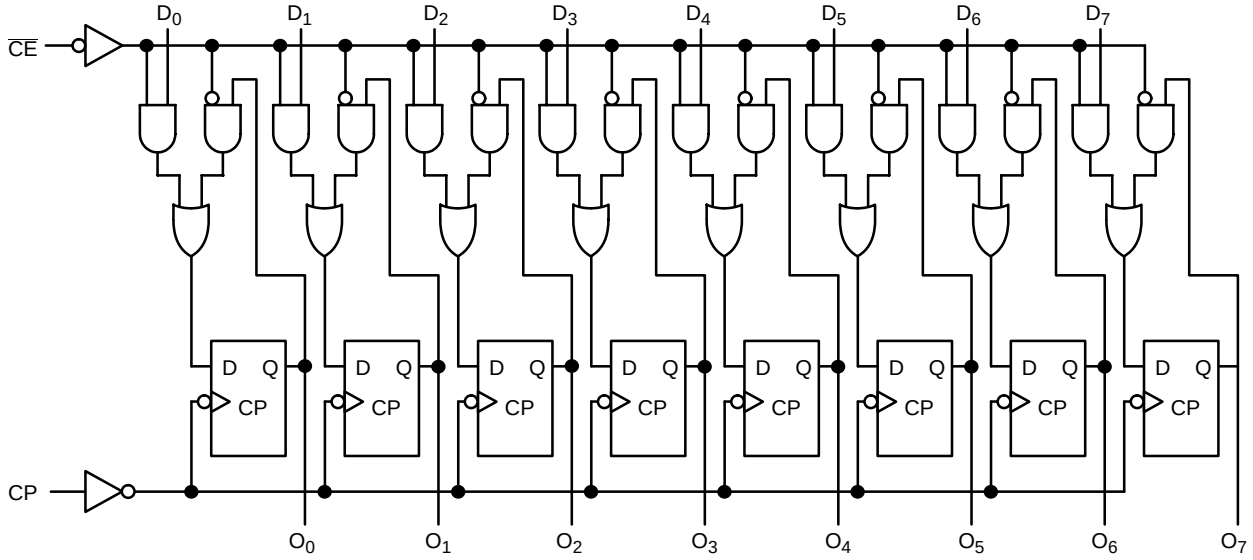
PIN NAMES

PIN	FUNCTION
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load ′1′	⌐	L	H	H
Load ′0′	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. LOGIC DIAGRAM

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)		–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)		–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin		±20	mA
I_{out}	DC Output Sink/Source Current, per Pin		±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin		±50	mA
T_{stg}	Storage Temperature		–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	SOIC, DW TSSOP, DT PDIP, N	97 129 69	°C/W
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 > 1000	V
$I_{Latch–Up}$	Latch–Up Performance	V_{CC} = 5.5 V; TA = 125°C (Note 4)	> 100	mA

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

1. Tested to EIA/JESD22–A114–A
2. Tested to EIA/JESD22–A115–A
3. Tested to JESD22–C101–A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 5) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V		150		ns/V
		V_{CC} @ 4.5 V		40		
		V_{CC} @ 5.5 V		25		
t_r, t_f	Input Rise and Fall Time (Note 6) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V		10		ns/V
		V_{CC} @ 5.5 V		8.0		
T_J	Junction Temperature (PDIP)				140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current — High				–24	mA
I_{OL}	Output Current — Low				24	mA

5. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
6. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

74AC – DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = –40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.50 2.25 2.75	2.10 3.15 3.85	2.10 3.15 3.85	V V V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.50 2.25 2.75	0.90 1.35 1.65	0.90 1.35 1.65	V V V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V V V	I_{OUT} = –50 μA
		3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V V V	*V_{IN} = V_{IL} or V_{IH} –12 mA I_{OH} –24 mA –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V V V	I_{OUT} = 50 μA
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V V V	*V_{IN} = V_{IL} or V_{IH} –12 mA I_{OH} –24 mA –24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD} I_{OHD}	Maximum Input Leakage Current	5.5 5.5			75 –75	mA mA	V_{OLD} = 1.65 V Max V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.
NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

74AC – AC CHARACTERISTICS For Figures and Waveforms, See Figures 4, 5, and 6.

Symbol	Parameter	V_{CC}* (V)	T_A = +25°C C_L = 50 pF			T_A = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	90 140			75 125		MHz
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0		13.0 9.0	1.5 1.5	14.0 10.0	ns
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	3.5 2.5		13.0 10.0	2.0 1.5	14.5 11.0	ns

* Voltage Range 3.3 V is 3.3 V ±0.3 V; Voltage Range 5.0 V is 5.0 V ±0.5 V.

74AC – AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	T_A = +25°C C_L = 50 pF	T_A = –40°C to +85°C	Unit
			Typ	Guaranteed Minimum	
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0		5.5 4.0	6.0 4.5	ns
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0		0 1.0	0 1.0	ns
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0		6.0 4.0	7.5 4.5	ns
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0		0 1.0	0 1.0	ns
t_w	CP Pulse Width HIGH or LOW	3.3 5.0		5.5 4.0	6.0 4.5	ns

* Voltage Range 3.3 V is 3.3 V ±0.3 V; Voltage Range 5.0 V is 5.0 V ±0.5 V.

74ACT – DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = –40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = –50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} –24 mA I_{OH} –24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} –24 mA I_{OH} –24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} – 2.1 V
I_{OLD} I_{OHD}	†Minimum Dynamic Output Current	5.5			75 –75	mA	V_{OLD} = 1.65 V Max V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

74ACT – AC CHARACTERISTICS For Figures and Waveforms — See Figures 4, 5, and 6.

Symbol	Parameter		V_{CC}* (V)	T_A = +25°C C_L = 50 pF			T_A = –40°C to +85°C C_L = 50 pF		Unit
				Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency		5.0	140			125		MHz
t_{PLH}	Propagation Delay	CP to Q_n	5.0	3.0		9.0	2.5	10	ns
t_{PHL}	Propagation Delay	CP to Q_n	5.0	3.5		10	2.5	11	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

74ACT – AC OPERATING REQUIREMENTS

Symbol	Parameter		V_{CC}* (V)	T_A = +25°C C_L = 50 pF		T_A = –40°C to +85°C C_L = 50 pF	Unit
				Typ	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW	D_n to CP	5.0		4.5	5.5	ns
t_h	Hold Time, HIGH or LOW	D_n to CP	5.0		1.0	1.0	ns
t_s	Setup Time, HIGH or LOW	$\overline{CE}$ to CP	5.0		4.5	5.5	ns
t_h	Hold Time, HIGH or LOW	$\overline{CE}$ to CP	5.0		1.0	1.0	ns
t_w	CP Pulse Width	HIGH or LOW	5.0		4.0	4.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	90	pF	V_{CC} = 5.0 V

SWITCHING WAVEFORMS

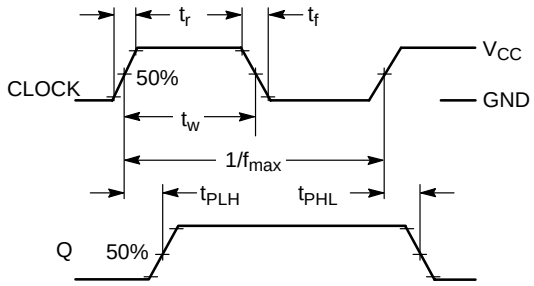


Figure 4.

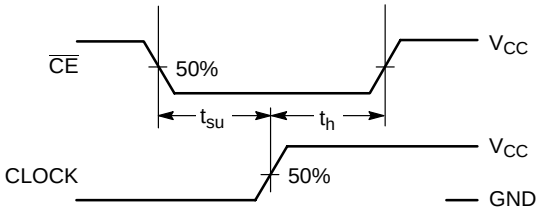


Figure 5.

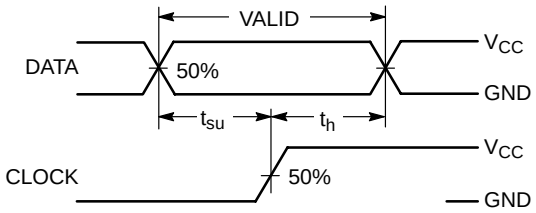
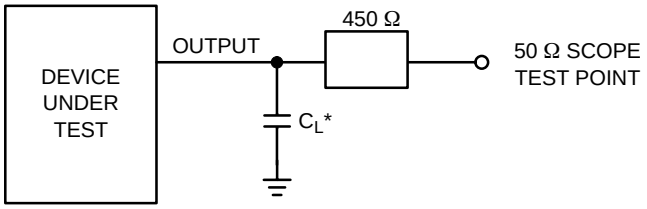


Figure 6.



*Includes all probe and jig capacitance

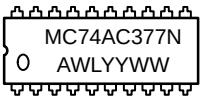
Figure 7. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping
MC74AC377N	PDIP–20	18 Units/Rail
MC74ACT377N	PDIP–20	18 Units/Rail
MC74AC377DW	SOIC–20	38 Units/Rail
MC74AC377DWR2	SOIC–20	1000 Tape & Reel
MC74ACT377DW	SOIC–20	38 Units/Rail
MC74ACT377DWR2	SOIC–20	1000 Tape & Reel
MC74AC377DT	TSSOP–20	75 Units/Rail
MC74AC377DTR2	TSSOP–20	2500 Tape & Reel
MC74ACT377DT	TSSOP–20	75 Units/Rail
MC74AC377M	EIAJ–20	40 Units/Rail
MC74ACT377M	EIAJ–20	40 Units/Rail
MC74ACT377MEL	EIAJ–20	2000 Tape & Reel

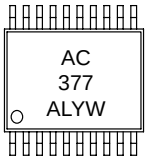
MARKING DIAGRAMS

PDIP–20



SO–20

TSSOP–20



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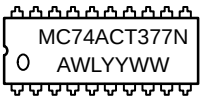
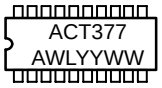
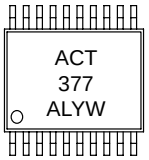


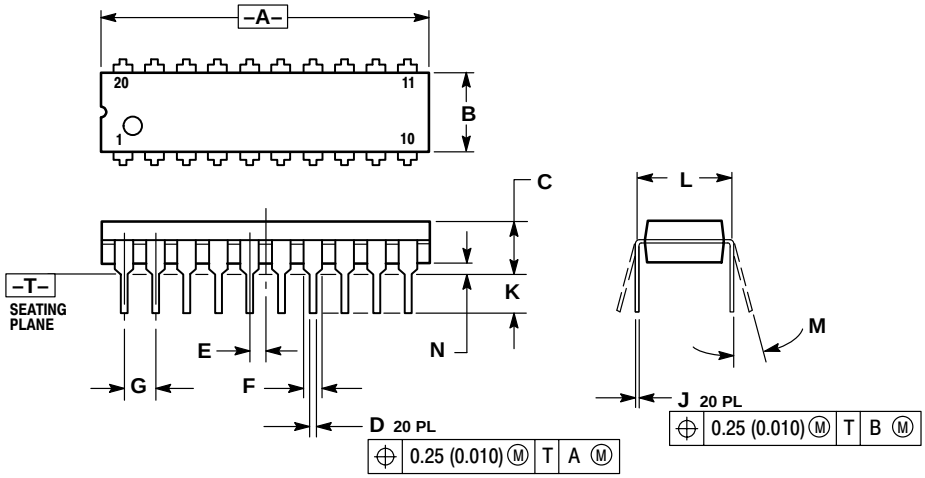




A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

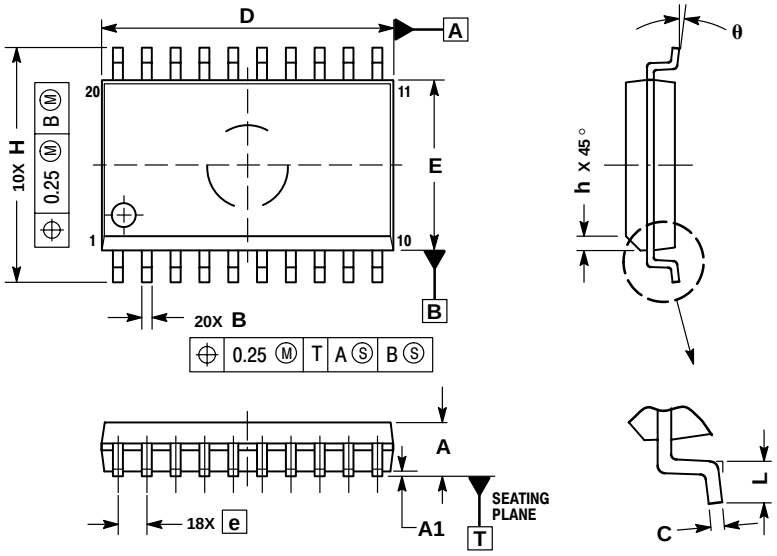
PDIP–20
N SUFFIX
20 PIN PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO–20
DW SUFFIX
20 PIN PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F

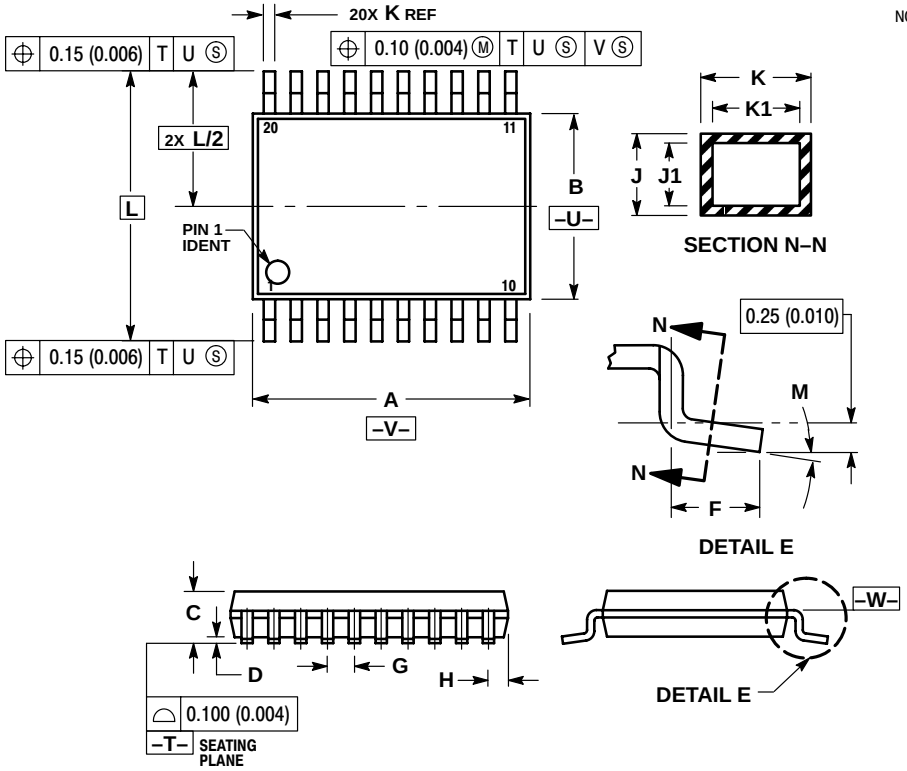


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE DIMENSIONS

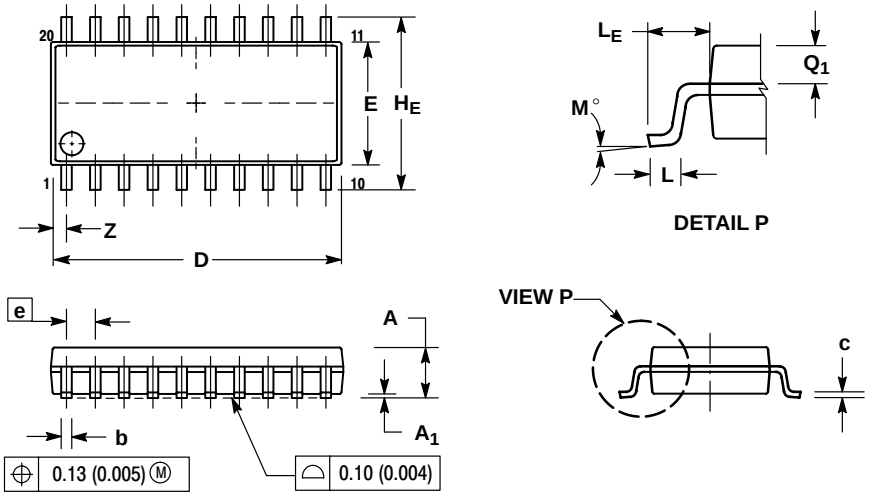
TSSOP–20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

EIAJ–20
M SUFFIX
20 PIN PLASTIC EIAJ PACKAGE
CASE 967–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

Notes

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